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10/075,656	02/13/2002	Detlev Richter	P2001,0097	9370

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,656	RICHTER, DETLEV	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/13/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *021302*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 have been examined.

Drawings

2. The drawings are objected to because descriptive labels other than numerical are needed for figures 1-3. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The examiner would like to point out that method claims are typically illustrated by a simple flowchart(s) with the boxes containing the steps of the method. These drawings aid in the understanding of the claimed invention.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: There are multiple typographical errors concerning hyphenated words which have the space after the hyphen. An example of this error would be for "self- test" on page 5 line 23. All occurrences should be corrected. Appropriate correction is required.

Claim Objections

5. Claim 1 is objected to because of the following informalities: The phrase "a plurality bidirectionally operating interface circuits" should read "a plurality of bidirectionally operating interface circuits". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 2:

The specification does not describe an additional circuit (fourth circuit) "for receiving and processing test signals received via said interface circuit of said first group." Rather, the specification discloses that both groups are connected to the common MISR 30. (Page 11, lines 10-14). Correction is required.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1-13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim recites the limitation "the mutually assigned interface circuits" on lines 8 and 9. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-13:

These claims are rejected because they depend on claim 1 and contain the same problems of insufficient antecedent basis.

Claim 7:

This claim is rejected as being a hybrid claim because it recites a method claim, which is inconsistent with the previous structure claim (claim1).

Claim 11:

This claim recites the limitation "selecting from the group consisting of..." on lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 8-13:

These claims are rejected because they depend on claim 7 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 7, 9, 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanghani (US-2003/0101376), hereinafter Sanghani, in view of Zumkehr (US-2003/0120989), hereinafter Zumkehr.

Claims 1 and 7:

Sanghani teaches a macro cell is provided for a DDR I/O interface (e.g., for an integrated circuit) which provides built-in self-testability, operable at the normal data rate of the interface, and may be combined with similar cells (first and second equally sized groups) to form an I/O interface of suitable size. Sanghani teaches a BIST controller is also provided for an I/O interface where a relatively slow JTAG controller (according to IEEE 1149.1) may initiate self-testing (electrical connection...for enabling self-test) through the BIST controller. (Page 2, ¶ 7, 20, Fig. 8). Sanghani also teaches a linear feed back shift register (LFSR) (a first circuit...serving to generate test signals) is employed to generate DDR patterns for testing the DDR output logic. Sanghani further teaches the test patterns produced by LFSR 200 are applied to the DDR I/O interface (e.g., macro cell 100 of FIG. 1A) and then received at the evaluation/result circuitry of FIG. 1B (second circuit...for receiving and processing test signals), through receive buffer 124, for comparison with the original test DDR signal patterns (comparing the received tests signals with prescribed values) and error generation (calculating a signature). Sanghani suggests that transmit buffer 122, receive buffer 124 and bump 126 may, collectively, comprise bi-directional High-Speed Transceiver Logic (HSTL

BIDI) (plurality of bi-directionally operating interface circuits). (Page 2, ¶ 30,31). Sanghani does not explicitly teach a separate voltage supply for the first and second groups of interface circuits. However, Zumkehr suggests the utilization of well-known power/ground connections in the testing of double date rate (DDR) devices. (Page 1, ¶ 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify Sanghani's voltage supply configuration to use Zumkehr's well-known power/ground connections in the testing of double date rate (DDR) devices. The artisan would have been motivated to do so because this would enable Sanghani to separately connect the several groups of I/O interface circuits for better power distribution.

Claim 2:

Sanghani teaches a linear feed back shift register (LFSR) (a third circuit...serving to generate test signals) is employed to generate DDR patterns for testing the DDR output logic. Sanghani also teaches the test patterns produced by LFSR 200 are applied to the DDR I/O interface (e.g., macro cell 100 of FIG. 1A) and then received at the evaluation/result circuitry of FIG. 1B (fourth circuit...for receiving and processing test signals), through receive buffer 124, for comparison with the original test DDR signal patterns and error generation. (Page 2, ¶ 31).

Claims 3 and 4:

Sanghani teaches a linear feed back shift register (LFSR) (pseudorandom number generator of claim 3) is employed to generate DDR patterns for testing the DDR output logic.

Claim 5:

Sanghani teaches the test patterns produced by LFSR 200 are applied to the DDR I/O interface (e.g., macro cell 100 of FIG. 1A) and then received at the evaluation/result circuitry of FIG. 1B (fourth circuit...for receiving and processing test signals), through receive buffer 124, for comparison with the original test DDR signal patterns and error generation (calculating a signature). (Page 2, ¶ 31).

Claim 8:

Sanghani teaches in FIG. 8, I/O BIST controller 802 drives the input/output at its operating frequency. DDR transmit macro cells 820a-820n and DDR receive macro cells 830a-830n generate test patterns (reverse a test direction), compare them with what the I/O interface produces in response to the patterns and return a result signal (e.g., bistFlag).

Claim 9:

Sanghani teaches a linear feed back shift register (LFSR) (generating test signals) is employed to generate DDR patterns for testing the DDR output logic. Sanghani further teaches the test patterns produced by LFSR 200 are applied to the DDR I/O interface (e.g., macro cell 100 of FIG. 1A) and then received at the evaluation/result circuitry of FIG. 1B (second circuit...for receiving and processing test signals), through receive buffer 124, for comparison with the original test DDR signal patterns (comparing the signature with prescribed signature) and error generation (calculating a signature).

Claim 10:

Sanghani teaches a BIST controller is also provided for an I/O interface where a relatively slow JTAG controller (according to IEEE 1149.1) may initiate self-testing (influencing a connection of the assigned interface circuit) through the BIST controller. (Page 2, ¶ 7, 20, Fig. 8).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanghani (US-2003/0101376), hereinafter Sanghani, in view of Zumkehr (US-2003/0120989), hereinafter Zumkehr, and further in view of Takagi (US-6704897), hereinafter Takagi.

Claim 6:

Sanghani does not explicitly teach a multiple input shift register (MISR) fro receiving and processing test signals. However, Sanghani does teach the test patterns produced by LFSR 200 are applied to the DDR I/O interface and then received at the evaluation/result circuitry of FIG. 1B (circuit for receiving and processing test signals), through receive buffer 124, for comparison with the original test DDR signal patterns and error generation. Takagi teaches a compaction circuit 13 (MISR) for compacting random data. (Col. 5, lines 31-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani's evaluation/result circuitry with Takagi compaction circuit 13 (MISR). The artisan would have been motivated to do so because this would enable Sanghani's evaluation/result circuitry to further evaluate consecutively store the resulting random data Takagi's flip flop 70'.

10. Claim 11-13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanghani (US-2003/0101376), hereinafter Sanghani, in view of Zumkehr (US-2003/0120989), hereinafter Zumkehr, and further in view of Levy et al. (US-5751151), hereinafter Levy.

Claim 11:

Sanghani does not explicitly teach of the influencing step consisting of resistive, capacitive and inductive. However, Levy suggests when VDD potential is to be applied to the corresponding pin of the DUT 10A and 10B, a corresponding relay coil, such as the relay coil 30 (inductive influence), is operated to pull the contact 26 from its lower position to its upper position, where it then is attached to a source or operating potential (VDD) as illustrated in FIG. 1. (Col. 4, lines 28-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani testing method to include Levy's method of applying VDD influences via the corresponding relay coils. The artisan would have been motivated to do so because this would give Sanghani more flexibility in applying power sources to the DDR I/O interface circuits during testing.

Claim 12:

Sanghani does not explicitly teach of modulating low-frequency signal voltages onto the supply voltages. However, Levy suggests when VDD potential is to be applied to the corresponding pin of the DUT 10A and 10B, a corresponding relay coil, such as the relay coil 30 (inductive influence), is operated to pull the contact 26 from its lower position to its upper position, where it then is attached to a source or operating potential

(VDD) as illustrated in FIG. 1. (Col. 4, lines 28-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani testing method to include Levy's method of applying VDD influences via the corresponding relay coils. The artisan would have been motivated to do so because this would give Sanghani more flexibility in applying power sources to the DDR I/O interface circuits during testing.

Claim 13:

Sanghani does not explicitly teach of modulating two low-frequency sinusoidal signals. However, Levy suggests when VDD potential is to be applied to the corresponding pin of the DUT 10A and 10B, a corresponding relay coil, such as the relay coil 30 (inductive influence), is operated to pull the contact 26 from its lower position to its upper position, where it then is attached to a source or operating potential (VDD) as illustrated in FIG. 1. (Col. 4, lines 28-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanghani testing method to include Levy's method of applying VDD influences via the corresponding relay coils. The artisan would have been motivated to do so because this would give Sanghani more flexibility in applying power sources to the DDR I/O interface circuits during testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
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